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10/067,890	02/08/2002	Takeyuki Suzuki	04208.0136	8020

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EXAMINER
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ALANKO, ANITA KAREN

ART UNIT	PAPER NUMBER
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1765

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DATE MAILED: 10/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/067,890

Applicant(s)

SUZUKI ET AL.

Examiner

Anita K Alanko

Art Unit

1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 February 2002 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_ 6) ☐ Other:

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***Drawings***

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the wiring patterns, conductive patterns, and the relative position of the substrate (and substrate features of through holes and patterns) with respect to the KGD (as in claims 2, 6 and 7) must be shown or the features canceled from the claims. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 112***

*Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.*

In claims 1, 6 and 7, line 1, the term "substrate for KGD" is unclear. Does the substrate act as a bare chip carrier for a KGD, or is the substrate the same as the KGD?

As to claims 1, 6 and 7, the relative surfaces are unclear. The specification defines the surfaces as front and rear surfaces, but the claims do not, and it is therefore unclear how the surfaces all relate to each other.

In claim 6, the terms "one surface" and "a surface" in lines 6 and 7 lack proper antecedent basis. Are these surfaces different from the "both surfaces" cited in lines 2-3?

Claims 2-5 do not cure the indefiniteness of their base claim, and are therefore also rejected.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

*Claims 1-4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art in view of Nagano et al (JP 07-211750 A).*

Admitted prior art discloses a method for forming a recognition mark on a substrate as a bare chip carrier for a KGD, wherein wiring patterns 2 are formed on a surface of one side of an insulating substrate 1 (the front surface in Figure 5A), comprising the steps of:

forming a conductive pattern as a recognition mark 6 on the rear surface (Fig.6B); and  
forming a through hole 3 from a surface where said wiring pattern is not formed toward the front surface (Fig.5A).

Admitted prior art does not disclose that the recognition mark and the wiring patterns are formed on the same surface (the front surface). Admitted prior art also does not disclose that the through hole is formed from the rear surface toward a recognition mark on the front surface.

Nagano teaches a method comprising forming recognition marks 5,7 from the same material as that for wiring patterns 4 (abstract, lines 20-24). Using the same material for both

recognition marks and wiring patterns saves material, which in turn saves process steps, time and money, since multiple materials and multiple depositing steps do not need to be conducted.

It would have been obvious to one with ordinary skill in the art to form the recognition marks and the wiring patterns on the same, front surface in the method of admitted prior art because Nagano teaches that this is a useful technique for forming recognition marks and wiring patterns, and because it saves time and money to form them at the same time on the same surface.

Nagano also teaches that it is useful to have recognition marks include through holes 6 (abstract, line 24 and Figure 2). Admitted prior art discloses forming through holes from a rear surface towards the front surface (page 2, lines 24-27).

It would have been still further obvious to form the through hole from the rear surface toward a recognition mark on the front surface in the modified method of admitted prior art because Nagano also teaches that through holes are useful to be formed in recognition mark layers, and since the recognition marks are present on the front surface in the modified method of admitted prior art, it is obvious to form the through holes toward them.

As to claim 2, admitted prior art discloses to form a bump 4 to be connected to said KGD on the surface where said wiring pattern is not formed (Fig.5B).

As to claim 3, admitted prior art discloses that recognition mark 6 (forming by coating and etching) has a particular shape as said recognition mark (Fig.6B).

As to claim 4, the modified method of admitted prior art teaches to have a through hole 6 that defines the recognition mark (Fig.2A-2B cross shape or circular shape).

As to claim 6, the modified method of admitted prior art does not teach to form a through hole from the front surface (where the KGD is not mounted). However, since the hole goes through the substrate, it would have been obvious to form the hole from either surface including the front surface in the modified method of admitted prior art since the same final product results.

*Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art in view of Nagano et al (JP 07-211750 A) and Appelt et al (US 6,015,520).*

The discussion of modified admitted prior art from above is repeated here.

As to claim 5, admitted prior art teaches that the bump 4 protrudes from the rear surface, not that it is flush with the surface. Appelt teaches that flush plated through holes 22' (Fig.4) are known alternatives for protrusions/bumps (Fig.3) in chip carriers (col.1, line 5).

It would have been obvious to one with ordinary skill in the art to form plating that is flush with the surface in the modified method of admitted prior art because Appelt teaches that this is a useful alternative for bumps in chip carriers.

*Claims 1-4 and 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art in view of Nagano et al (JP 07-211750 A) and Miura et al (JP 2000-165047 A).*

The discussion of modified admitted prior art from above is repeated here.

As to claim 7, admitted prior art teaches forming recognition marks on any layer where said wiring patterns are formed and forming a through hole from a surface of the substrate where

said KGD is to be mounted toward said conductive pattern. Admitted prior art does not explicitly teach forming wiring patterns on a plurality of layers.

Miura teaches that it is known to form a plurality of wiring layers 12 and recognition mark layers 4 (Figures 1, 2 and 4). It would have been obvious to one with ordinary skill in the art to form wiring patterns on a plurality of layers in the modified method of admitted prior art because Miura teaches that it is useful to have a plurality of wiring layers to form a final product.

### *Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Brown is cited to show a method with flush plating. Nam is cited to show plating a recognition mark. Isaacs is cited to show a chip carrier. Fjelstad is cited to show a method of forming an interposer. Hashizume et al is cited to show recognition marks 5 and bumps 4 on the same surface of the substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anita K Alanko whose telephone number is 703-305-7708. The examiner can normally be reached on Monday, Tuesday and Friday, 8:00 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 703-305-2667. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

Application/Control Number: 10/067,890

Page 7

Art Unit: 1765

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*Anita K. Alanko*

Anita K Alanko  
Primary Examiner  
Art Unit 1765